CLAIMS

1. A magnetic random access memory comprising, in combination:

a plurality of magnetic memory elements that perform a memory operation;

a word line to magnetically activate at least one magnetic memory element;

a sense line to detect the state of the at least one magnetic memory element;

a word line driver connected to the word line to drive a current on the word line during the memory operation; and

a word line equalizer connect to the word line to equalize the word line during non-memory operations.

2. The magnetic random access memory of claim 1 with the memory operation being a read operation.

3. The magnetic random access memory of claim 1 with the memory operation being a write operation

4. The magnetic random access memory of claim 1 with the word line driver further comprising, in combination:

a first transistor with a gate connected to an equalize signal and a first terminal connected to a power supply and a second terminal connected to a first end of the word line;

a second transistor connected to a second end of the word line, with the first transistor cooperating with the second transistor to drive current on the word line when the equalize signal is inactive; and

an equalizer transistor connected to provide a equalization signal to the word line when the equalize signal is active.

5. The magnetic random access memory of claim 1 with the word line having a first half word line and a second half word line, with a word line select switch connected between the first half word line and the second half word line.

6. The magnetic random access memory of claim 1 further comprising, in combination: a plurality of word lines.

7. The magnetic random access memory of claim 1 further comprising, in combination: a plurality of word lines, each one of the plurality of word lines having a first half word line and a second half word line, with the first half word line and the second half

word line connected to a word line select switch that selects at least one of the plurality of word lines.

8. The magnetic random access memory of claim 1 further comprising, in combination: a word line controller that enables the word line equalizer in response to a word line enable signal.

9. The magnetic random access memory of claim 1 further comprising, in combination:

a plurality of word lines; and

an address bus to select the magnetic memory element with one of the plurality of word lines and the address bus.

10. The magnetic random access memory of claim 1 with the word line driver further comprising, in combination:

a logic controller having a read/write input, an enable input, and a read enable output and a write enable output; and

a feedback amplifier having a sense reference read signal input, a sense reference write signal input, a word line signal input, and a word line driver signal output, with the feedback amplifier providing current to the word line in response to the read enable output and the write enable output.

11. The magnetic random access memory of claim 10 with the current in the word line being a '1' direction.

12. The magnetic random access memory of claim 10 with the current in the word line being in a '0' direction.

13. The magnetic random access memory of claim 10 with the current in the word line being controlled during MRAM testing.

14. A current controlled word current source for a magnetic random access memory comprising, in combination:

a current source having a stable reference current output; and

a word current source having a word current reference input connected to the stable reference current output with the word current source having a word current output.

15. A word line driver for a word line in a magnetic random access memory comprising, in combination:

a logic controller having a read/write input, an enable input, and a read enable output and a write enable output; and

a feedback amplifier having a sense reference read signal input, a sense reference write signal input, a word line signal input, and a word line driver signal output, with the feedback amplifier providing current to the word line in response to the read enable output and the write enable output.

16. The word line driver of claim 15 with the current in the word line being in a '1' direction.

17. The word line driver of claim 15 with the current in the word line being in a '0' direction.

18. The word line driver of claim 15 with the current in the word line being controlled during MRAM testing.

19. The word line driver of claim 15 further comprising, in combination:

a test controller connected to a first word line driver to test a second word line driver; and

an external pad to allow off chip detection of a signal on the second word line driver.

20. The word line driver of claim 19 with the signal being a word line current.